CLAIMS

What is claimed is:

1. A method of forming an integrated circuit chip having at least one opening in a substrate, said method comprising:

forming an opening having vertical walls in said substrate;

protecting a first portion of said vertical walls of said opening, leaving a second portion of said vertical walls unprotected; and

laterally patterning said second portion of said opening to change a property of said opening.

2. The method in claim 1, wherein said laterally patterning comprises one of an isotropic wet etch, an isotropic dry etch and an anisotropic wet etch.

3. The method in claim 1, wherein said protecting comprises forming a mask over said first portion of said vertical walls.

4. The method in claim 1, wherein said first portion comprises one of an upper and a lower portion of said opening.

5. The method in claim 1, wherein said first portion and said second portion comprises alternating portions along a length of said opening.

6. A method of forming an integrated circuit chip having at least one opening in a substrate, said method comprising:

forming an opening having vertical walls in said substrate;

protecting a first portion of said vertical walls of said opening, leaving a second portion of said vertical walls unprotected; and

laterally patterning said second portion of said opening to form a step in said opening.

7. The method in claim 6, wherein said laterally patterning comprises one of an isotropic wet etch, an isotropic dry etch and an anisotropic wet etch.

8. The method in claim 6, wherein said protecting comprises forming a mask over said first portion of said vertical walls.

9. The method in claim 6, wherein said first portion comprises a lower portion of said opening.

10. The method in claim 6, wherein said substrate comprises a semiconductor and said method further comprises doping selected portions of said step to form two conductive regions separated by a semiconductive region,

wherein in the presence of an adjacent voltage field, said semiconductive region changes its conductivity and performs a switching operation in combination with said conductive regions.

11. A method of forming an integrated circuit chip having at least one transistor, said method comprising:

forming an opening having vertical walls in a semiconductor substrate;

protecting a first portion of said vertical walls of said opening, leaving a second portion of said vertical walls unprotected;

laterally patterning said second portion of said opening to form a step in said opening; and

doping selected portions of said step to form two conductive regions separated by a semiconductive region,

wherein in the presence of an adjacent voltage field, said semiconductive region changes its conductivity and performs a switching operation in combination with said conductive regions.

12. The method in claim 11, wherein said laterally patterning comprises one of an isotropic wet etch, an isotropic dry etch and an anisotropic wet etch.

13. The method in claim 11, wherein said protecting comprises forming a mask over said first portion of said vertical walls.

14. The method in claim 11, wherein said first portion comprises a lower portion of said opening.

15. A method of forming an integrated circuit chip having at least one opening in a substrate, said method comprising:

forming an opening having vertical walls in said substrate;

protecting first portions of said vertical walls of said opening, leaving second portions of said vertical walls unprotected, wherein said first portions alternate with said second portions; and

laterally patterning said second portions of said opening to change a property of said opening.

16. The method in claim 15, wherein said laterally patterning comprises one of an isotropic wet etch, an isotropic dry etch and an anisotropic wet etch.

17. The method in claim 15, wherein said protecting comprises forming a mask over said first portions of said vertical walls.

18. The method in claim 15, further comprising, after said laterally patterning, lining said opening with an insulator and filling a remainder of said opening with a conductor to form a deep trench capacitor.

19. The method in claim 15, further comprising, after said laterally patterning:

forming a gate insulator in said second portions;

forming a gate conductor over said gate insulator in said second portions;

doping said first portions to form source and drain regions; and

forming isolation regions over said source and drain regions.

20. The method in claim 19, wherein said gate insulator, said gate conductor, said source and drain regions and said isolation regions comprise a vertical transistor.

21. An integrated circuit having at least one trench capacitor, said trench capacitor comprising:

an opening having vertical sides, said vertical sides including a plurality of lateral openings;

an insulator lining said opening; and

a conductor filling said opening.

22. The integrated circuit in claim 21, wherein said lateral openings comprise rectangular openings in cross-section.

23. The integrated circuit in claim 21, wherein said lateral openings comprise v-shaped openings in cross-section.

24. The integrated circuit in claim 21, wherein said lateral openings comprise rounded openings in cross-section.

25. The integrated circuit in claim 21, wherein said lateral openings increase a surface area of said trench capacitor.

26. The integrated circuit in claim 21, wherein said lateral openings increase a capacitance of said trench capacitor.